IN THE CLAIMS

Please amend claim 1 and add the following new claims.

1. (Currently Amended) A method of designing a plurality of integrated circuits (ICs), said method comprising:

partitioning a technology independent RTL (register transfer level) netlist between said plurality of ICs which includes a first IC and a second IC and wherein said first IC is to be implemented in a first vendor specific technology and said second IC is to be implemented in a second vendor specific technology.

Claims 2-137. (Canceled)

138. (New) A method as in claim 1 further comprising:

compiling a hardware description language (HDL) code, wherein said technology independent RTL netlist is produced after compiling said HDL code.

139. (New) A method as in claim 138 wherein said ICs each comprise a programmable logic device and wherein said partitioning comprises assigning a portion of said technology independent RTL netlist to one of said plurality of ICs.

140. (New) A method as in claim 138 further comprising:

mapping said technology independent RTL netlist to a selected technology architecture.

141. (New) A method as in claim 140 wherein said mapping is performed after said partitioning.

142. (New) A method as in claim 140 further comprising:

performing a place and route operation after said mapping to implement said ICs in said selected technology architecture.

143. (New) A method as in claim 140 further comprising:
optimizing a design of each of said ICs after said partitioning.

144. (New) A method as in claim 143 wherein said optimizing optimizes each of said ICs by removing duplicative logic or input/outputs.

145. (New) A method as in claim 140 wherein said HDL code is created without regard to said partitioning.

146. (New) A method as in claim 143 wherein said optimizing and said mapping are performed after said partitioning.

147. (New) A method as in claim 140 further comprising:
mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

148. (New) A method as in claim 140 further comprising:
optimizing interconnects between modules of said technology independent RTL netlist before said partitioning.

149. (New) A method as in claim 147 wherein said estimates are used to decide how to perform said partitioning.

150. (New) A method as in claim 149 wherein a user considers said estimates and selects a command to decide how to perform said partitioning.

151. (New) A method as in claim 140 wherein said ICs each comprise a programmable logic device and wherein said method further comprises:

testing a prototype of a system with said ICs;

performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).

152. (New) A machine readable medium containing a plurality of executable instructions, which when executed on a digital processing system cause said digital processing system to perform a method of designing a plurality of integrated circuits (ICs), said method comprising:

partitioning a technology independent RTL (register transfer level) netlist between said plurality of ICs which includes a first IC and a second IC and wherein said first IC is to be implemented in a first vendor specific technology and said second IC is to be implemented in a second vendor specific technology.

153. (New) A machine readable medium as in claim 152, wherein said method further comprises:

compiling a hardware description language (HDL) code, wherein said technology independent RTL netlist is produced after compiling said HDL code.

154. (New) A machine readable medium as in claim 153 wherein said ICs each comprise a programmable logic device.

155. (New) A machine readable medium as in claim 153, wherein said method further comprises:

mapping said technology independent RTL netlist to a selected technology architecture.

156. (New) A machine readable medium as in claim 155 wherein said mapping is performed after said partitioning.

157. (New) A machine readable medium as in claim 155, wherein said method further comprises:

performing a place and route operation after said mapping to implement said ICs in said selected technology architecture.

158. (New) A machine readable medium as in claim 155, wherein said method further comprises:

optimizing a design of each of said ICs after said partitioning.

159. (New) A machine readable medium as in claim 158 wherein said optimizing optimizes each of said ICs by removing duplicative logic or input/outputs.

160. (New) A machine readable medium as in claim 155 wherein said HDL code is created without regard to said partitioning.

161. (New) A machine readable medium as in claim 158 wherein said optimizing and said mapping are performed after said partitioning.

162. (New) A machine readable medium as in claim 155, wherein said method further comprises:

mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

163. (New) A machine readable medium as in claim 155, wherein said method further comprises:

optimizing interconnects between modules of said technology independent RTL netlist before said partitioning.

164. (New) A machine readable medium as in claim 162 wherein said estimates are used to decide how to perform said partitioning.

165. (New) A machine readable medium as in claim 164 wherein a user considers said estimates and selects a command to decide how to perform said partitioning.

166. (New) A machine readable medium as in claim 155 wherein said ICs each comprise a programmable logic device and wherein said method further comprises:

testing a prototype of a system with said ICs;

performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).

167. (New) A system of designing a plurality of integrated circuits (ICs), said system comprising:

means for displaying a representation of said plurality of ICs;

means for partitioning a technology independent RTL (register transfer level) netlist between said plurality of ICs which includes a first IC and a second IC and

wherein said first IC is to be implemented in a first vendor specific technology and said second IC is to be implemented in a second vendor specific technology.

168. (New) A system as in claim 167 further comprising:

means for compiling a hardware description language (HDL) code, wherein said technology independent RTL netlist is produced after compiling said HDL code.

169. (New) A system as in claim 168 wherein said ICs each comprise a programmable logic device.

170. (New) A system as in claim 168 further comprising:

means for mapping said technology independent RTL netlist to a selected technology architecture.

171. (New) A system as in claim 170 wherein said mapping is performed after said partitioning.

172. (New) A system as in claim 170 further comprising:

means for performing a place and route operation after said mapping to implement said ICs in said selected technology architecture.

173. (New) A system as in claim 170 further comprising:

means for optimizing a design of each of said ICs after said partitioning.

174. (New) A system as in claim 173 wherein said optimizing optimizes each of said ICs by removing duplicative logic or input/outputs.

175. (New) A system as in claim 170 wherein said HDL code is created without regard to said partitioning.

176. (New) A system as in claim 173 wherein said optimizing and said mapping are performed after said partitioning.

177. (New) A system as in claim 170 further comprising:

means for mapping portions of said technology independent RTL netlist to a selected technology architecture wherein estimates of IC resources are obtained from said mapping portions and wherein said mapping portions is performed after said compiling and before said mapping.

178. (New) A system as in claim 170 further comprising:

means for optimizing interconnects between modules of said technology independent RTL netlist before said partitioning.

179. (New) A system as in claim 177 wherein said estimates are used to decide how to perform said partitioning.

180. (New) A system as in claim 179 wherein a user considers said estimates and selects a command to decide how to perform said partitioning.

181. (New) A system as in claim 170 wherein said ICs each comprise a programmable logic device and wherein said system further comprises:

means for testing a prototype of a system with said ICs;

means for performing a synthesis of said HDL code to generate at least one Application Specific Integrated Circuit (ASIC).